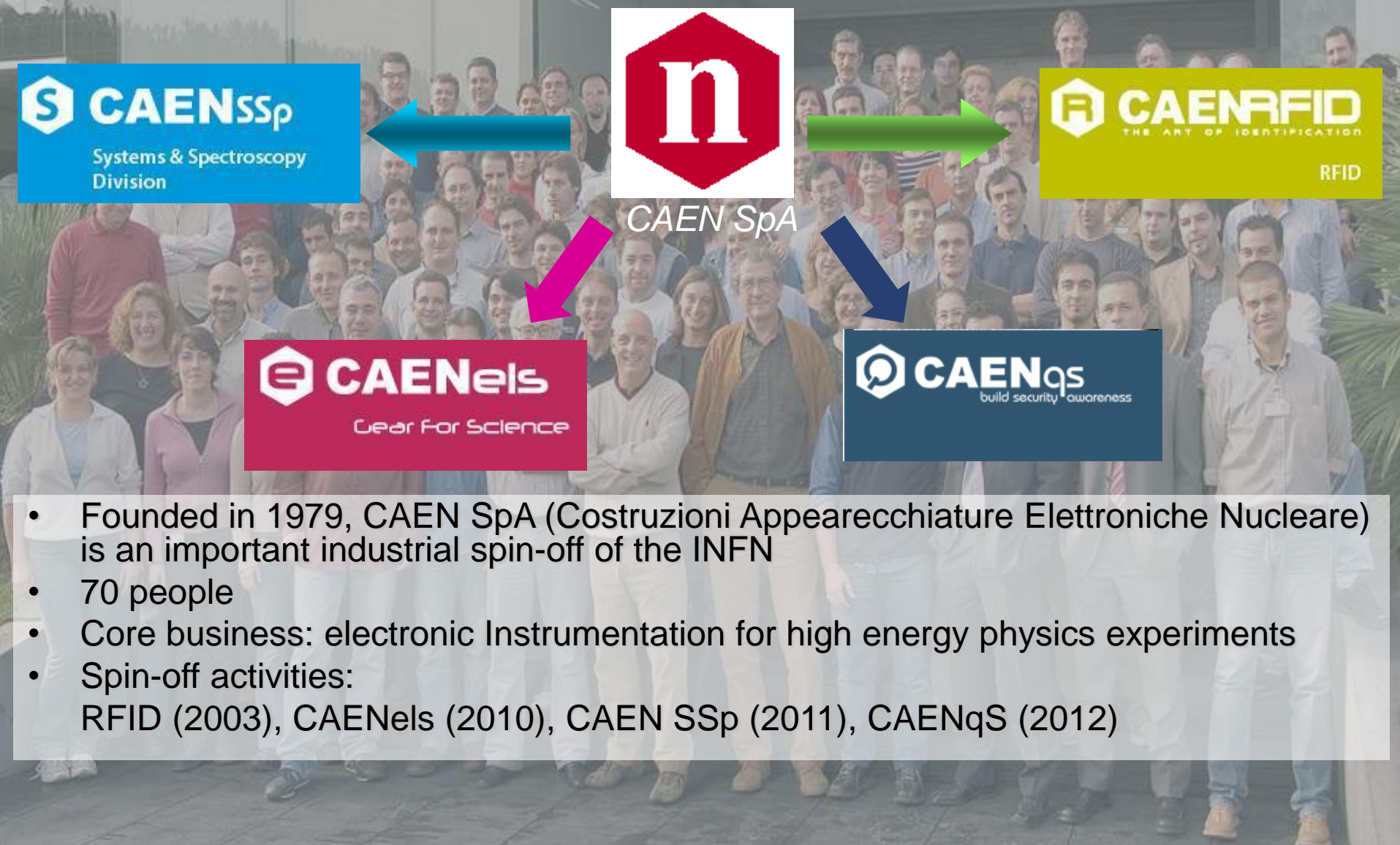


Digital Acquisition Instruments for Neutron Identification

Matteo Corbo

Design and Engineering of Neutron Instruments Meeting
7-9 September, 2015

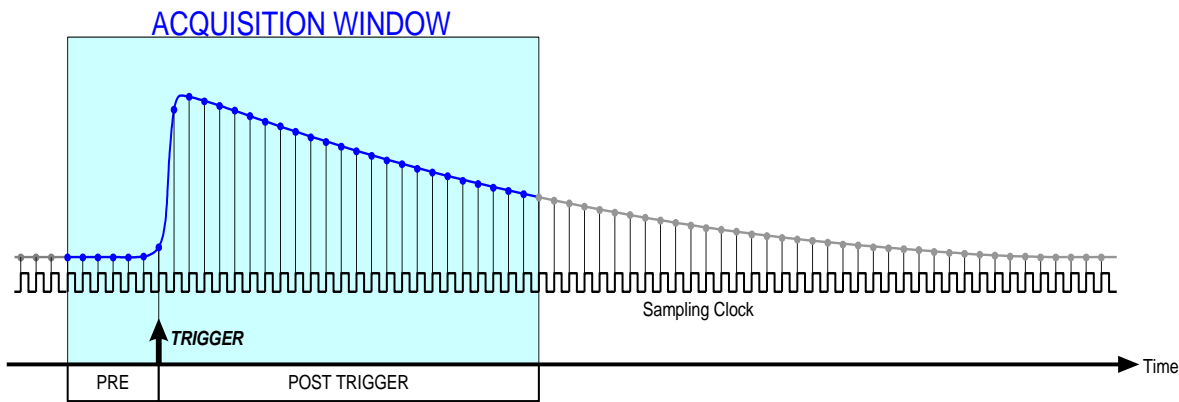


- 
- Worldwide sales network
 - CAEN offices in Italy, Germany, USA,
 - Distributors in all continents
 - Portfolio: >1000 customers
 - Customers Include world leading research centres:
 - Europe: CERN, INFN, GSI, ESO, ISIS, Ganil, PSI, ...
 - USA: FNAL, SLAC, Los Alamos, BNL, JLab, ...
 - Asia: J-Park, KEK, Riken, IHEP, TIFR, ...
 - Africa: iThemba Labs, ...
 - And private companies:
 - GE, Siemens, SAIC, L3, Raytheon, Lockheed

- **HV and LV Power Supplies for radiation and Low Light Sensors**
 - Multichannel CAEN Systems
 - Multichannel NIM and VME Modules
 - Compact Stand Alone Modules
- **Signal Conditioning & Read-out Electronics**
 - VME, NIM, CAMAC, Stand Alone Front-End/Data Acquisition Modules
 - Waveform digitizers
- **Powered Crates and Chassis**
- **Custom Developments**
- **Software User Interface**



- Digitizers as Oscilloscopes
 - Waveforms, time and voltage amplitude



Memory Buffer

TIME STAMP
S[0]
S[1]
S[2]
S[3]
⋮
S[n-1]

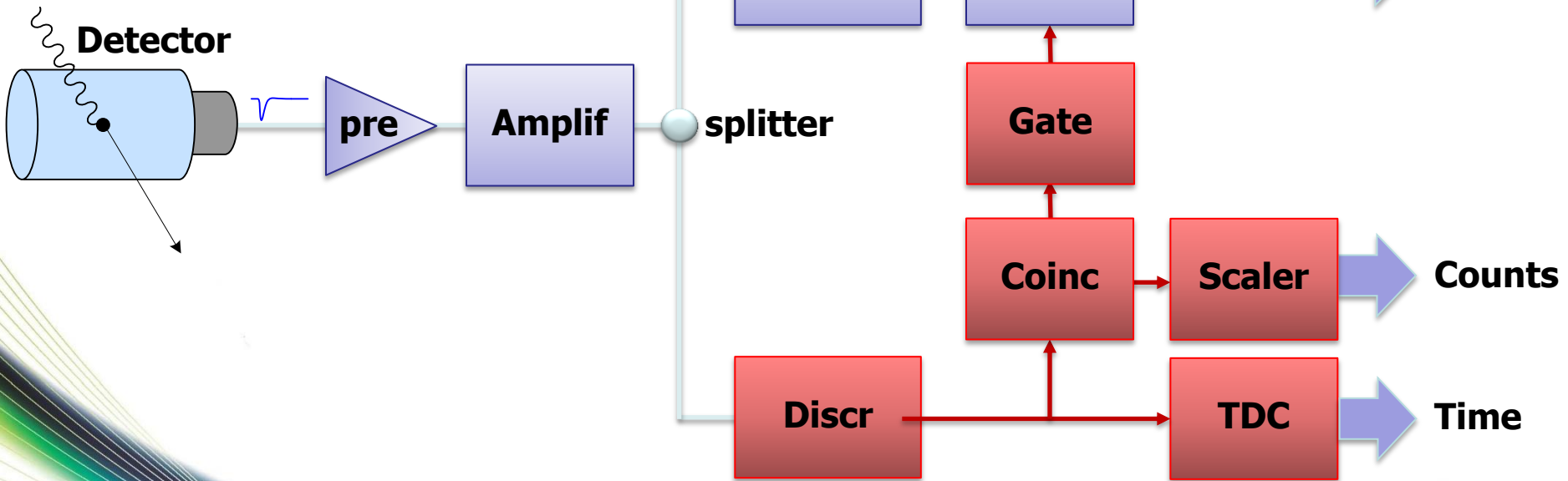


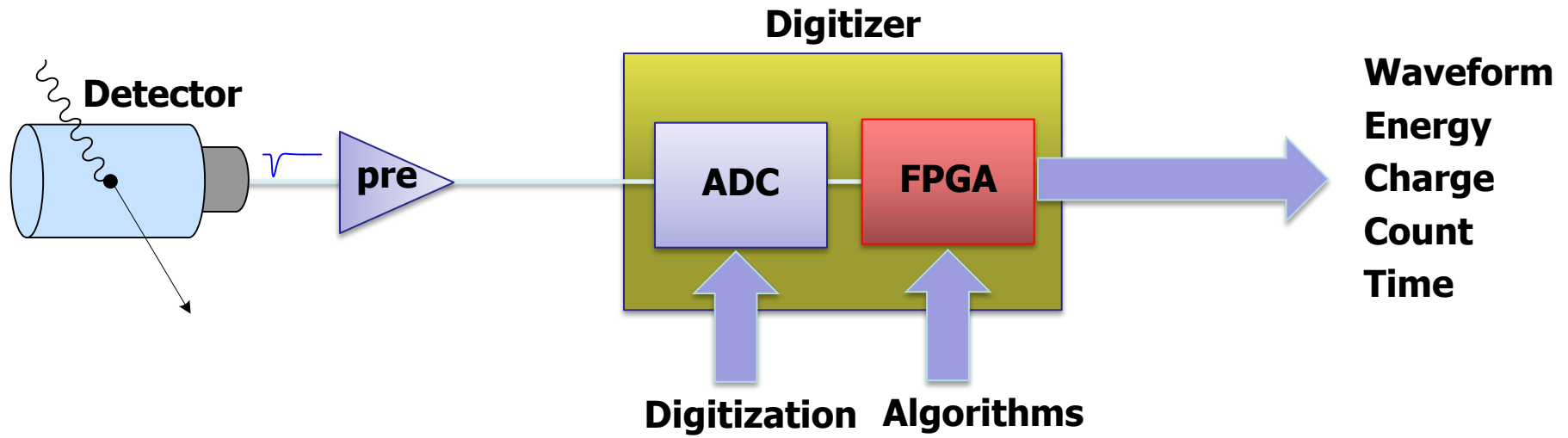
... and something more

- Onboard analysis through dedicated firmware algorithms
 - Designed for demanding data transfer
- Digitizers V.S. Analog acquisition systems
 - Real time and remote monitoring/setting
 - Adapt to detector upgrades
 - Waveform transfer, so room for later offline analysis
 - Different processing algorithms can be installed
 - Reduction in size, cabling, power consumption and cost per channel

A/D conversion at the end of the chain

Traditional acquisition chains are made of a number of analog modules interconnected with cables





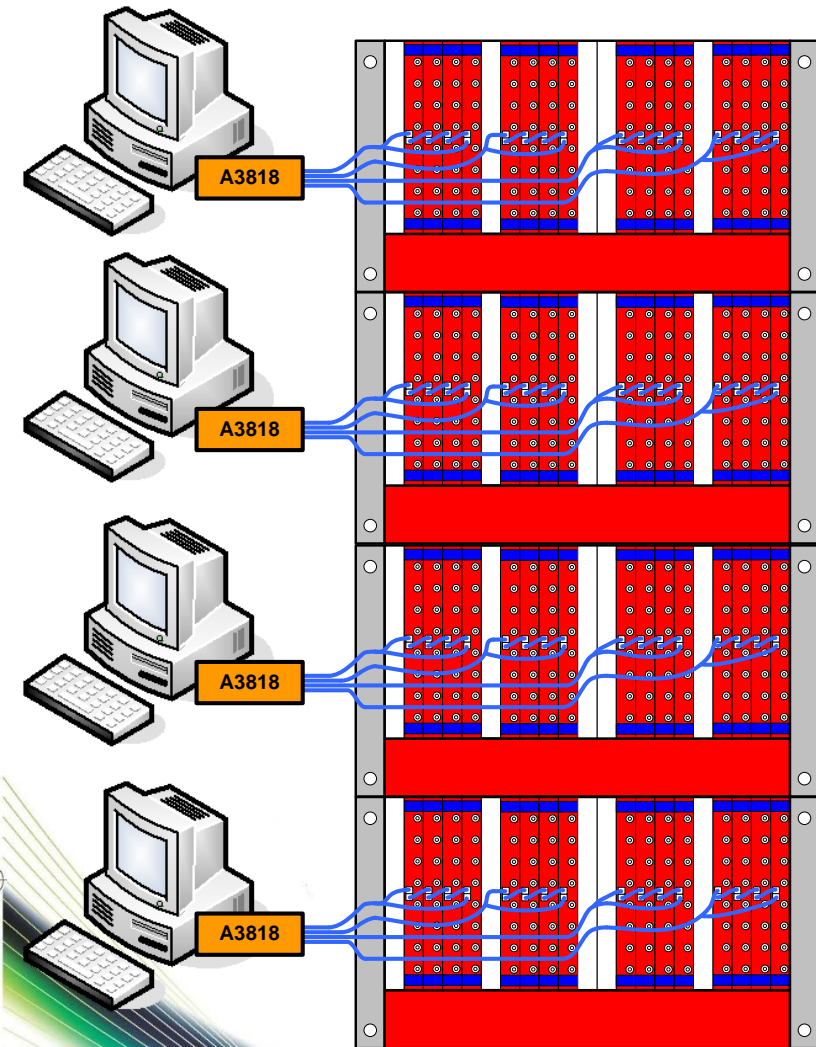
The aim of the Digital Pulse Processing is to make a “all in digital” version of analog modules such as Shaping Amplifiers, Discriminators, QDCs, Peak Sensing ADCs, TDCs, Scalers, Coincidence Units, etc.

- VME, NIM, Desktop form factors
 - VME64, VME64X compliant
- Hardware
 - FPGA firmware for Digital Pulse Processing
 - Interfaces: Optical Link (CONET), USB 2.0
 - Programmable digital I/Os on front panel
 - Memory buffers
- Multi-board synchronization and trigger distribution
 - Clock synthesis and distribution
 - Time stamp reset

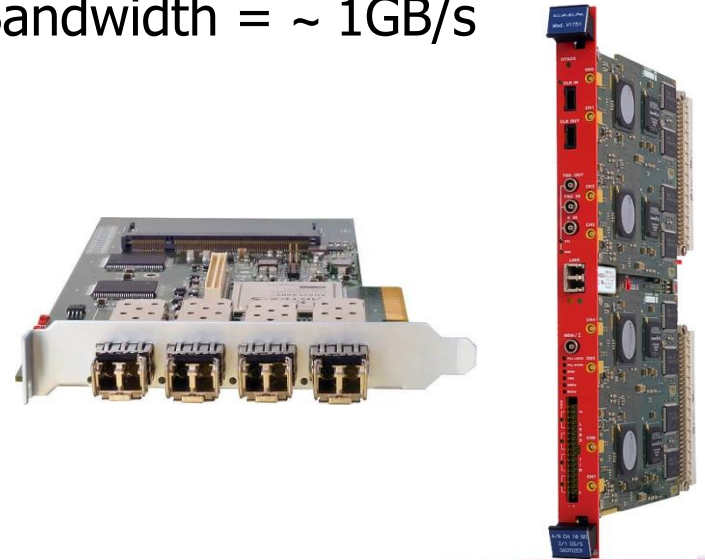


- **Proprietary protocol: Chainable Optical NETWORK**
- Benefits of fiber optics: long distance (>500m); no ground loop.
- **Daisy chain** (up to 8 boards) or point to point connection
- **Controllers:**
 - A2818 PCI (1 link)
 - A3818 PCIe (1, 2 or 4 links)
- VME Bridge also available, A2718
- Up to 80MB/s per link and up to 4 links per controller
- **Pros**
 - **High data throughput** without using VME bus communication
 - **High flexibility**, commercial computers as crate controllers





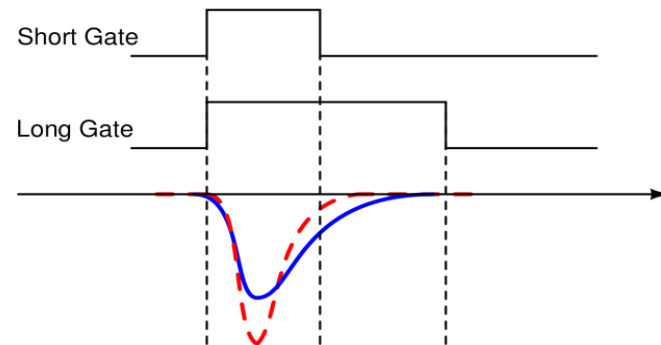
- 64 V1751 modules in 4 VME crates
- 512 channels (10 bit @ 1GHz)
- 4 A3818s 4 link PCIe cards
- 16 parallel CONET2 links
- 4 digitizers daisy chained
- Readout Bandwidth = ~ 2 MB/s/ch
- Total Bandwidth = ~ 1 GB/s



- **Standard Firmware**
 - Trigger on Leading Threshold
 - Waveforms, Time stamps
- **Digital Pulse Processing (DPP) Firmware**
 - Zero Length Encoding (**ZLE**) or Zero Suppression, to extract signal interest regions
 - Pulse Height Analysis (**PHA**) for spectroscopic applications
 - Charge Integration (**CI**), to measure particle released energy
 - **Pulse Shape Discrimination (PSD)**, to measure particle released energy and identify through the ionization density
 - On-board and real time analysis
 - Supporting **multiboard synchronization** and event correlation

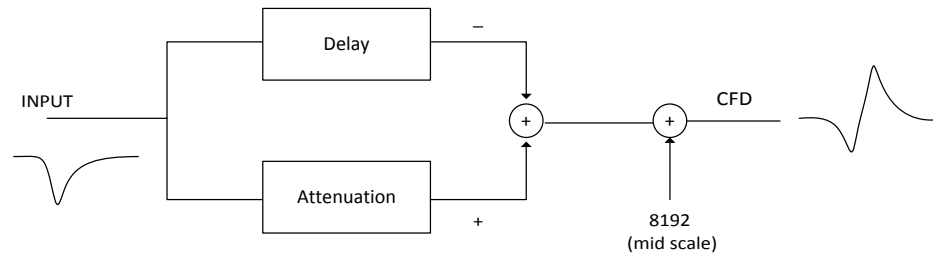
- Each channel is a **dual QDC + discriminator + gate generator**
- Dual gate integration for discriminating fast and slow components
- Pulse Shape Discrimination for n- γ separation

$$PSD = \frac{Q_{LONG} - Q_{SHORT}}{Q_{LONG}}$$

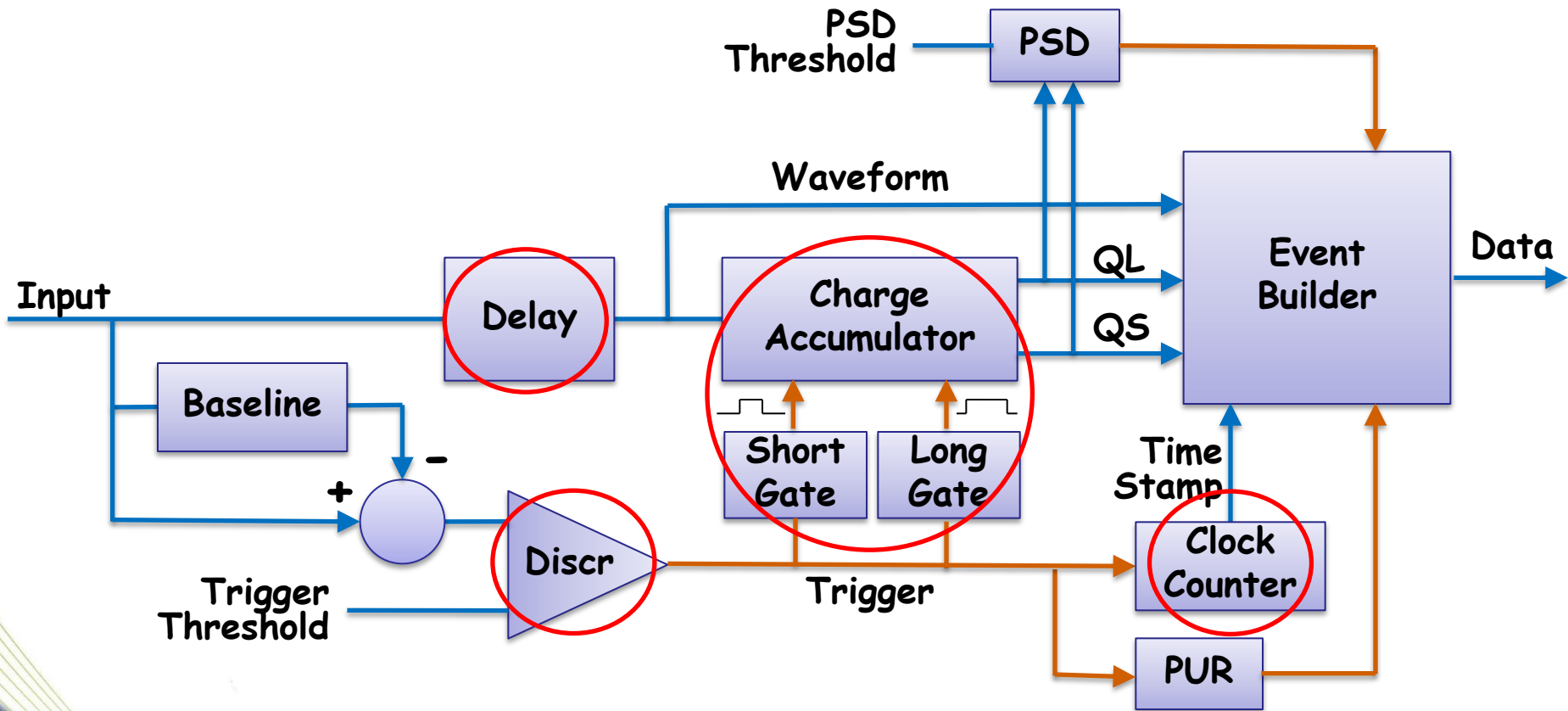


- Available for **x720** (12 bit @ 250MS/s), **x751** (10 bit @ 1GS/s) and **x730** (14 bit @ 500MS/s) and **DT5790** (2 channel 12 bit @ 250MS/s + 2 High Voltage + 2 Low Voltage for preamps)

- **Digital CFD** with time stamp interpolation (in x730, x751 families)



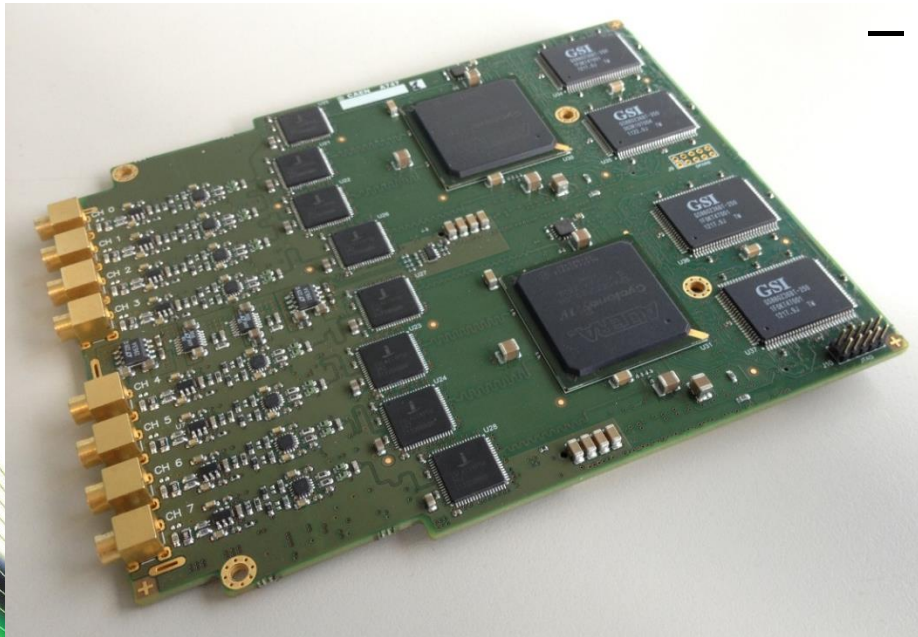
- **Improved measure of the time-of-flight**, possibly with sub nanosecond resolution
- **Pile-up rejection** or gate re-triggering
 - Reject false neutron signals, due to piling-up gammas
- **Online PSD cut to** reduce data throughput using a programmable PSD threshold (e.g. suppress gammas at high rates)
- Typically used with scintillators + PMT or SiPM/MPPC



Model ⁽¹⁾	Form Factor	N. of ch. ⁽²⁾	Max. Sampling Frequency (MS/s) ⁽²⁾	N. of Bits	Input Dynamic Range (Vpp) ⁽²⁾	Single Ended / Differential Input	Bandwidth (MHz) ⁽²⁾	Memory (MS/ch) ⁽²⁾
x720	VME	8	250	12	2	SE/D	125	1.25 / 10
	Desktop/NIM	4 / 2				SE		
x721	VME	8	500	8	1	SE/D	250	2
x724	VME	8	100	14	0.5 / 2.25 / 10	SE/D	40	0.5 / 4
	Desktop/NIM	4 / 2				SE		
x730	VME	16	500	14	0.5 - 2	SE	250	0.64 / 5.12
	NEW Desktop/NIM	8						
x731	VME	8 - 4	500 - 1000	8	1	SE/D	250 / 500	2 / 4
x740	VME	64	62.5	12	2 / 10	SE	30	0.19 / 1.5
	Desktop/NIM	32						
x751	VME	8 - 4	1000 - 2000	10	1	SE/D	500	1.8 - 3.6 / 14.4 - 28.8
	Desktop/NIM	4 - 2				SE		
x761	VME	2	4000	10	1	SE/D	1000	7.2 / 57.6
	Desktop/NIM	1				SE		
SWITCHED CAPACITOR x742	VME	32+2	5000 ⁽⁴⁾	12	1	SE	500	0.128 / 1
	Desktop/NIM	16+1						
NEW x743	VME	16	3200 ⁽⁴⁾	12	2.5	SE	500	0.007
	Desktop/NIM	8						

- **FADC**

- Solutions for multiple experimental applications
- Sampling frequency: from 62.5 MHz to 4 GHz
- Resolution up to 14 bits



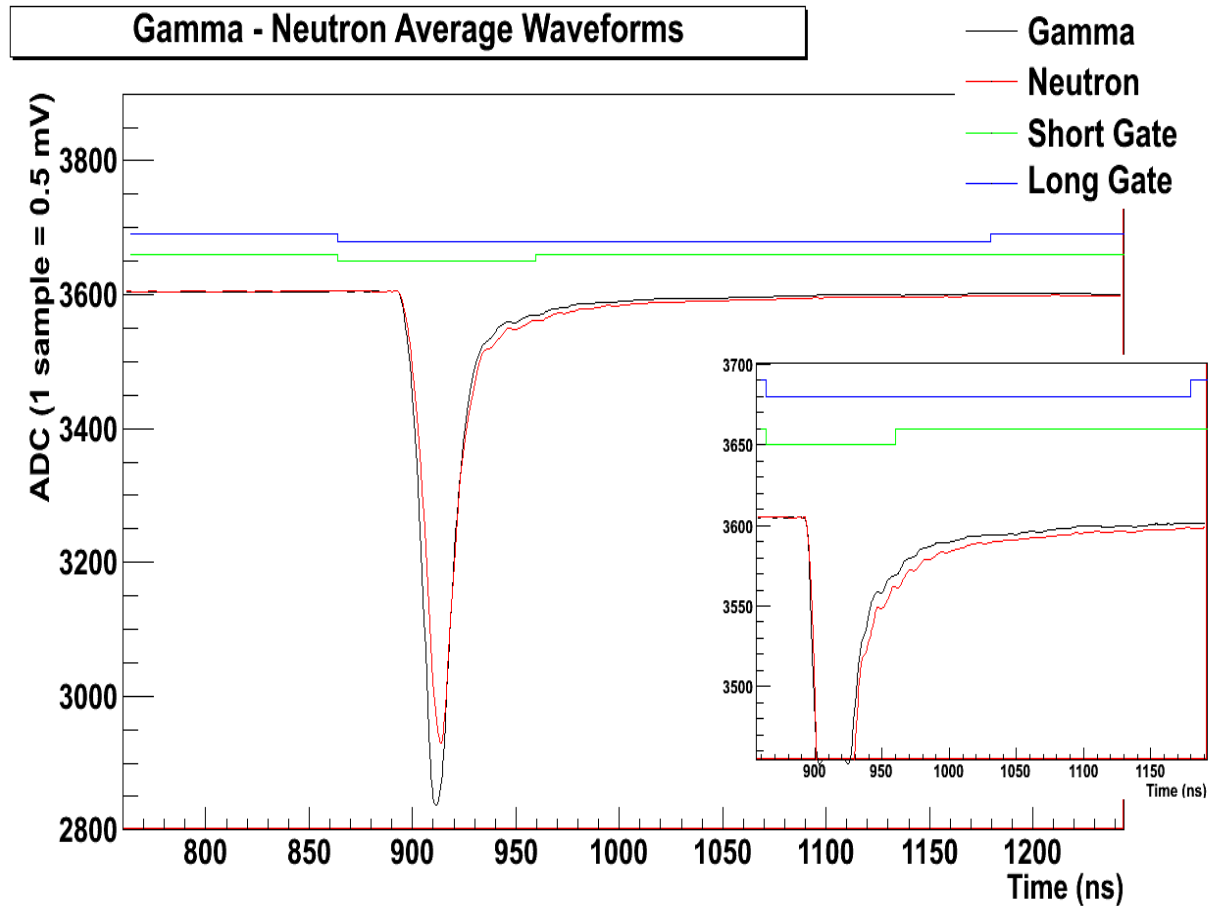
- Latest waveform digitizer: x730

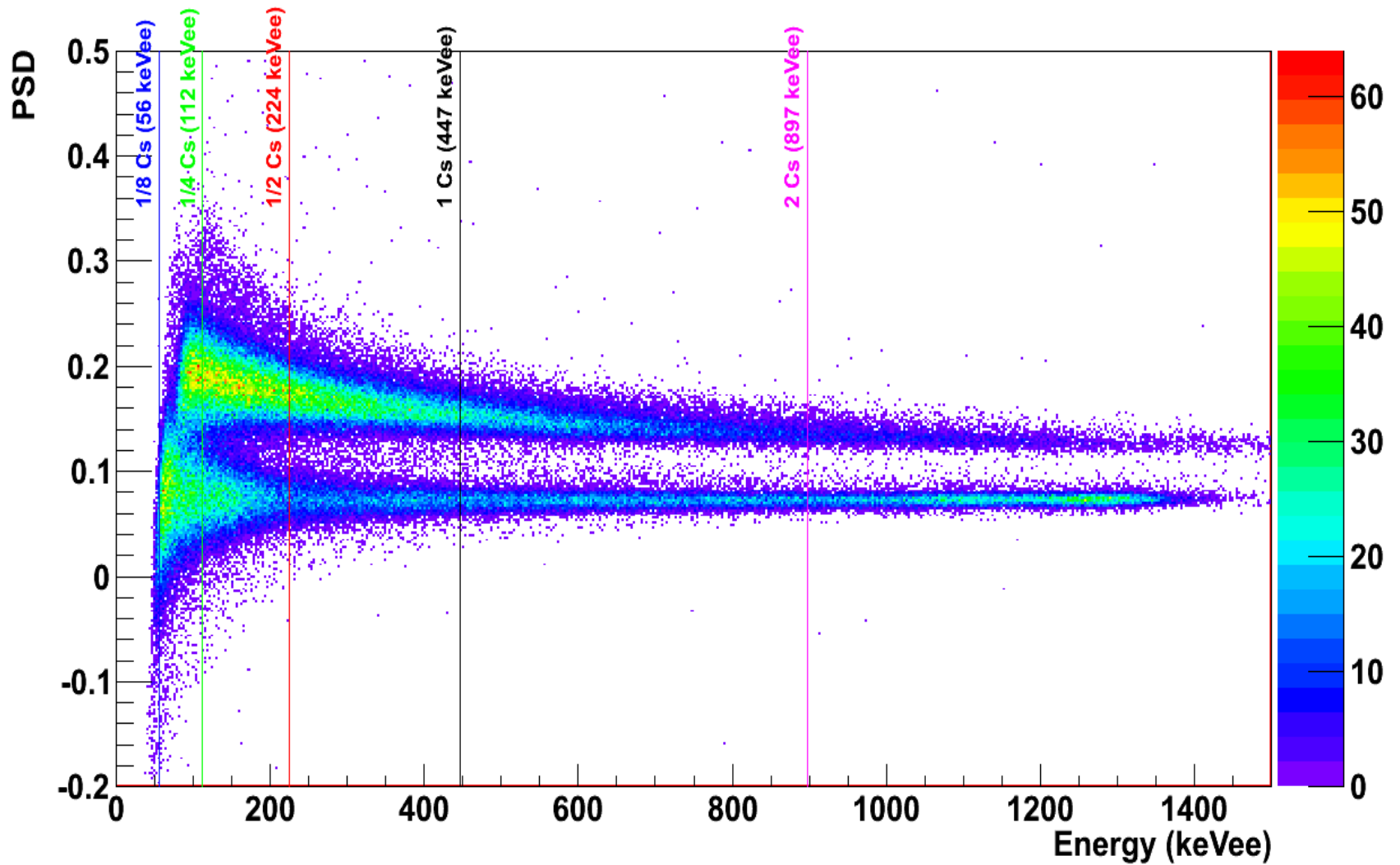
- Up to 16 channels in one board
- 500 MS/s, 250 MHz analog bandwidth, with 14 bits dynamic
- Double input dynamic range: 0.5 and 2 V_{pp} software set
- Available in VME, NIM and Desktop form factors
- Two firmware algorithms available

Detector: BC501A 5x2 inches,

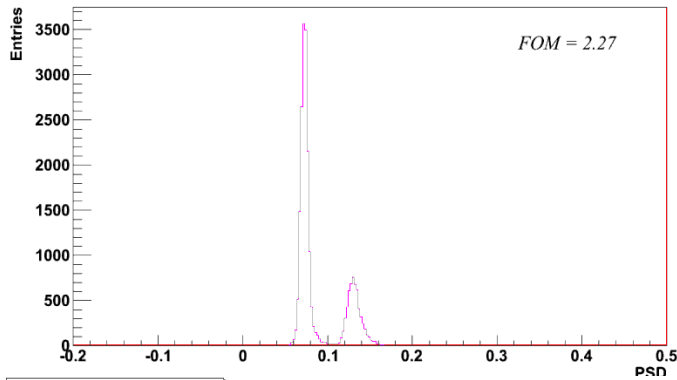
PMT: Hamamatsu R1250

Board: DT5720 with DPP-PSD

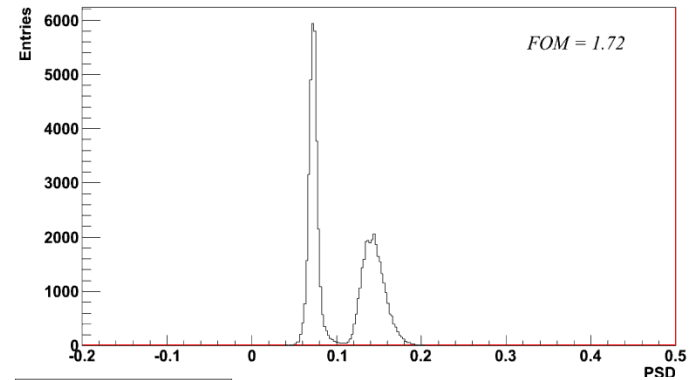




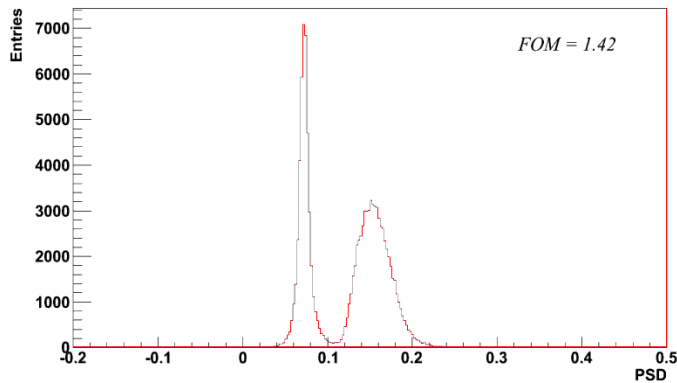
2 Cs (897 keVee)



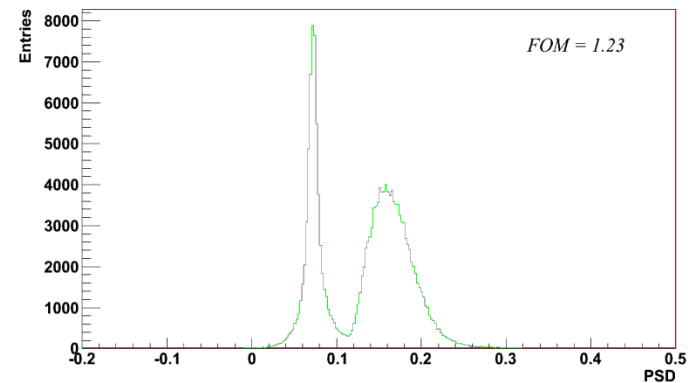
1 Cs (447 keVee)



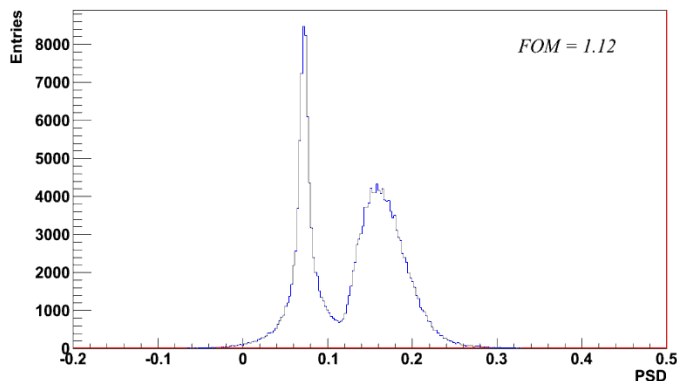
1/2 Cs (224 keVee)



1/4 Cs (112 keVee)

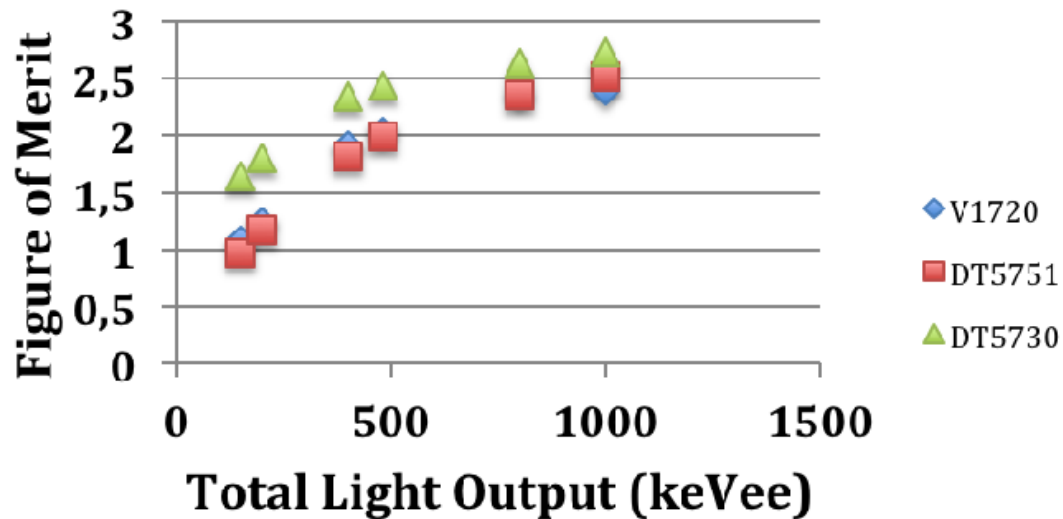


1/8 Cs (56 keVee)



$$FOM = \frac{\Delta PEAK}{FWHM_{\gamma} + FWHM_n}$$

DSP data, 1500 V, Cf source



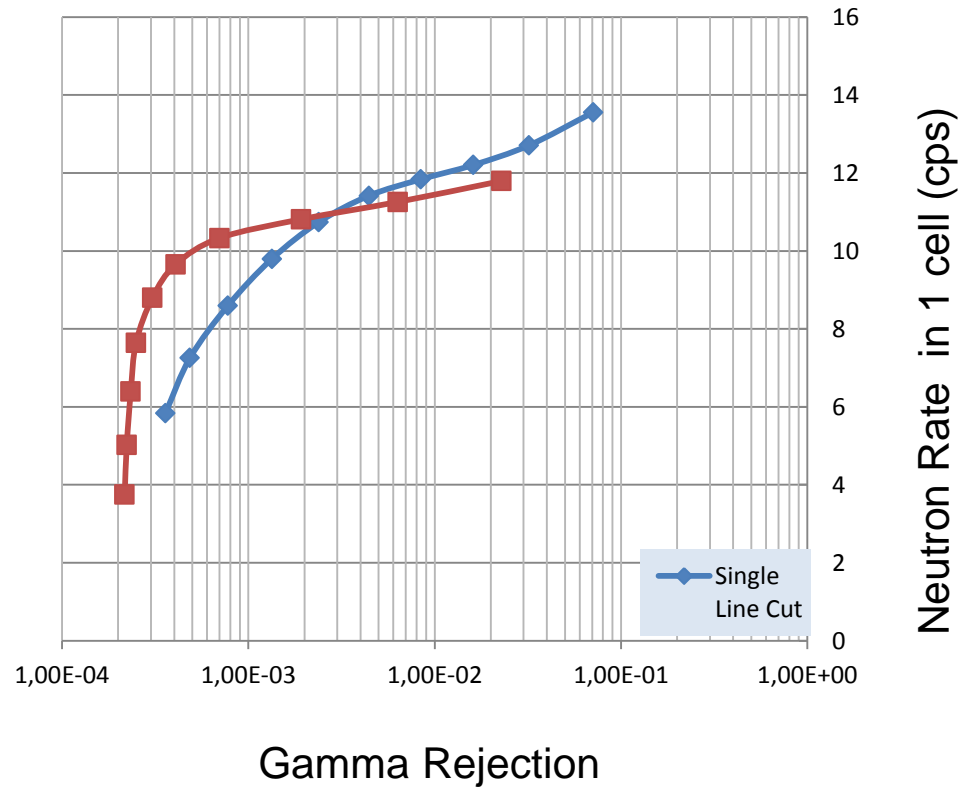
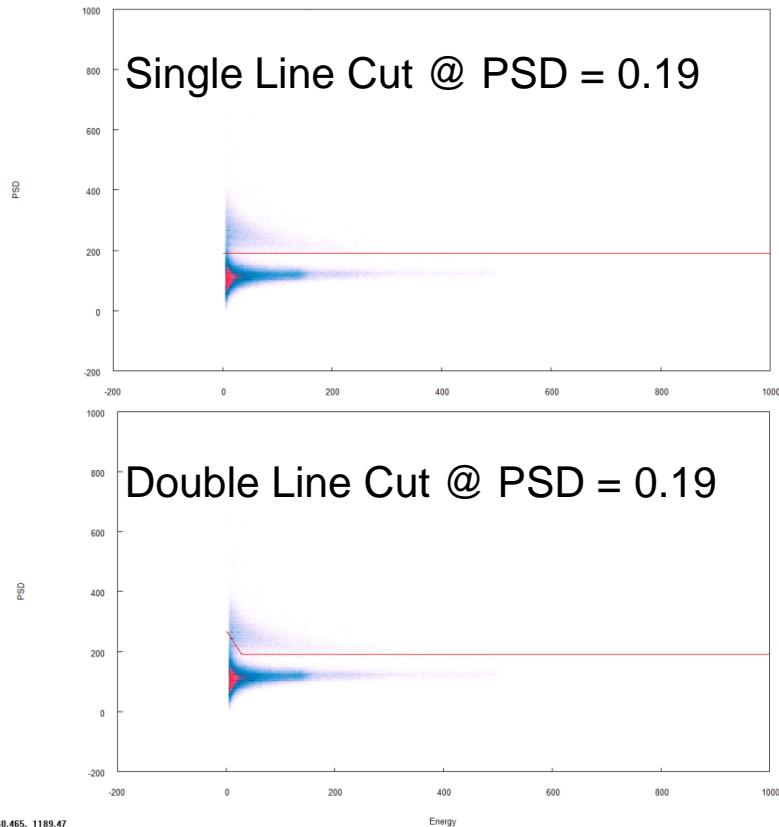
Tested families:

- **x720** (12 bit @ 250MS/s)
- **x751** (10 bit @ 1GS/s)
- **x730** (14 bit @ 500MS/s)

Detector: EJ309, volume ~ 1 liter

PMT: 9821FLB ET Enterprises

Board: DT5730 with DPP-PSD

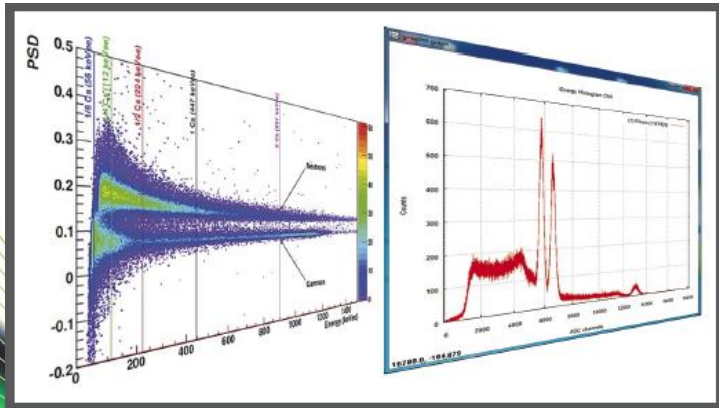


DT5790

Dual Charge-to-Digital Converter for Pulse Shape Discrimination



- Dual digital charge-to-digital converter based on 12-bit 250 MS/s FlashADCs
- Two HV power supply outputs rated up to ± 4 kV/3 mA
- Two DB9 connectors for preamplifier power supply
- USB and Optical Link communication interfaces
- Applications:
 - γ -n Discrimination
 - Spectroscopy with scintillators



EDEN European Funded Project Baggage scanning to identify fissile nuclear material

Acquisition system for ^3He or Boron tubes



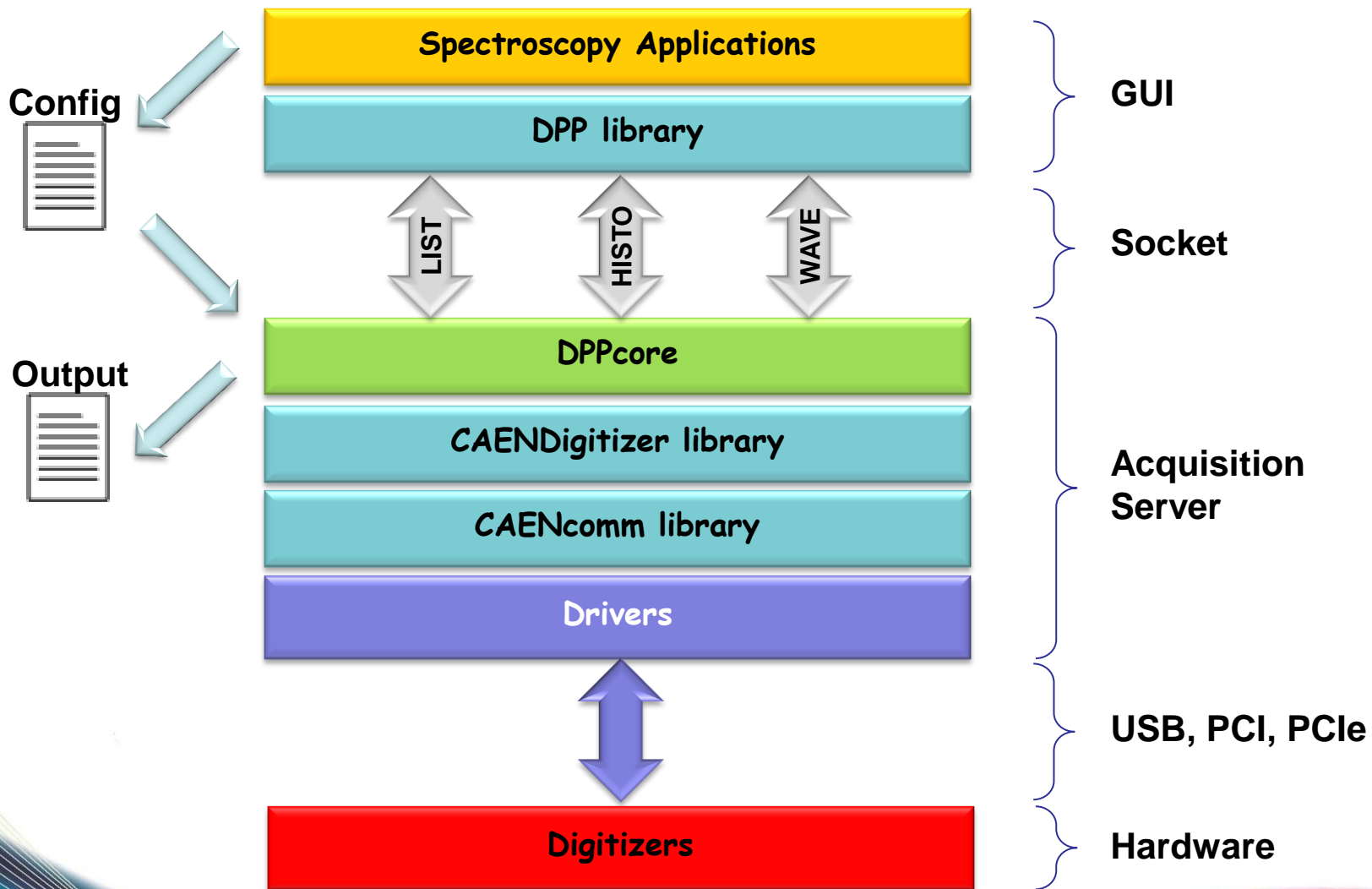
- 1 VME8004B Crate (Custom design)
- 1 V2718 VME Optical Link bridge
- 2 V6533 HV Boards
- 1 V1495 - General Purpose Board + 2 x 8 NIM/TTL I/O
- Control software

VME-USB bridge

Detector bias

Time stamp recording

- CAEN provides a **wide range of software tools** to configure and to control the data acquisition
 - Linux and Windows OS compatible (32 and 64 bits)
 - Free download
- **DRIVERS** for the communication channel:
 - CONET2 – optical link
 - VME bus
 - USB
- **LIBRARIES:**
 - C and LabView
 - Demo and examples available for developers
- **READOUT SOFTWARE:**
 - Medium and high level tools to manage the configuration and the data acquisition



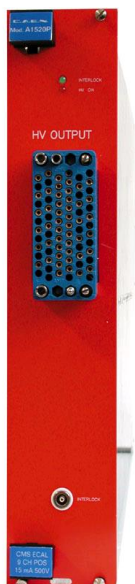
- Waveform digitizers are flexible and compact tools suitable for diverse applications
- On board data processing
 - replace at the same time different modules of a typical analog data acquisition chain
 - adapt to high rates
 - operate data reduction
 - may integrate event selection logic
- Fully exploit detector performances, comparable (and sometime better) with (than) analog acquisition chains

Backup

Power supply Systems

100% Compatible with all the power supply boards developed for the previous generation mainframes **SY1527/SY2527**

A1520P



A1533D



A1534

A2932



A1535 & A1550

A1526



A1510-A1511B
A1512-A1514B-A1519B

- Fully equipped experiment version
- 19" wide, 8U-high Euro-mechanics rack; depth: 720 mm, weight : 13kg
- 16 slots to house boards, distributors and branch controller
- Communications via Gigabit Ethernet and via Wi-Fi (optional)
- Local control via 10.4" color touchscreen LCD (optional)
- Fast, accurate setting and monitoring of channel parameters
- Modular and expandable power supply (up to 4 kW)
- Forced air cooling



- Small scale experiment and laboratory version
- 19" wide, 4U-high Euro-mechanics rack; depth: 700 mm
- 6 slots to house boards, distributors and branch controller
- Communications via Gigabit Ethernet and via Wi-Fi (optional)
- Local control via 5.7" colour touchscreen LCD (optional)
- Fast, accurate setting and monitoring of channel parameters
- Modular and expandable power supply (up to 1800 W)
- Forced air cooling



Modularity

- Chassis: SY4527, SY5527, SY4527LC, SY5527LC
- CPU Units: Basic, Advanced, Full
- Power Units: Primary, Boosters
- Accessories: LCD Touchscreen, Wi-Fi, Advanced SW

Connectivity

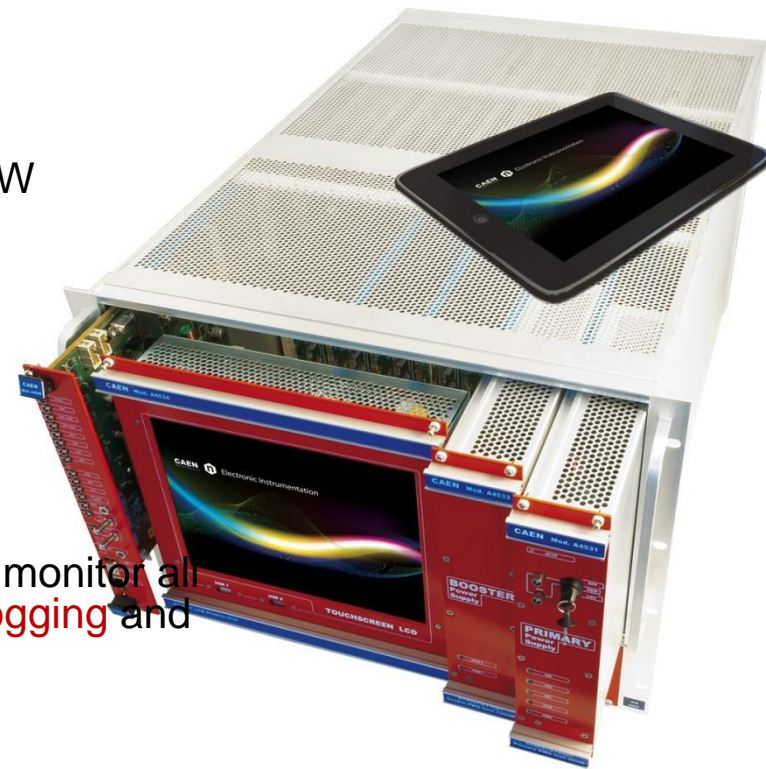
- Control based on new CPU modules either **Remote** via Ethernet and Wi-Fi or **Local** via touchscreen LCD

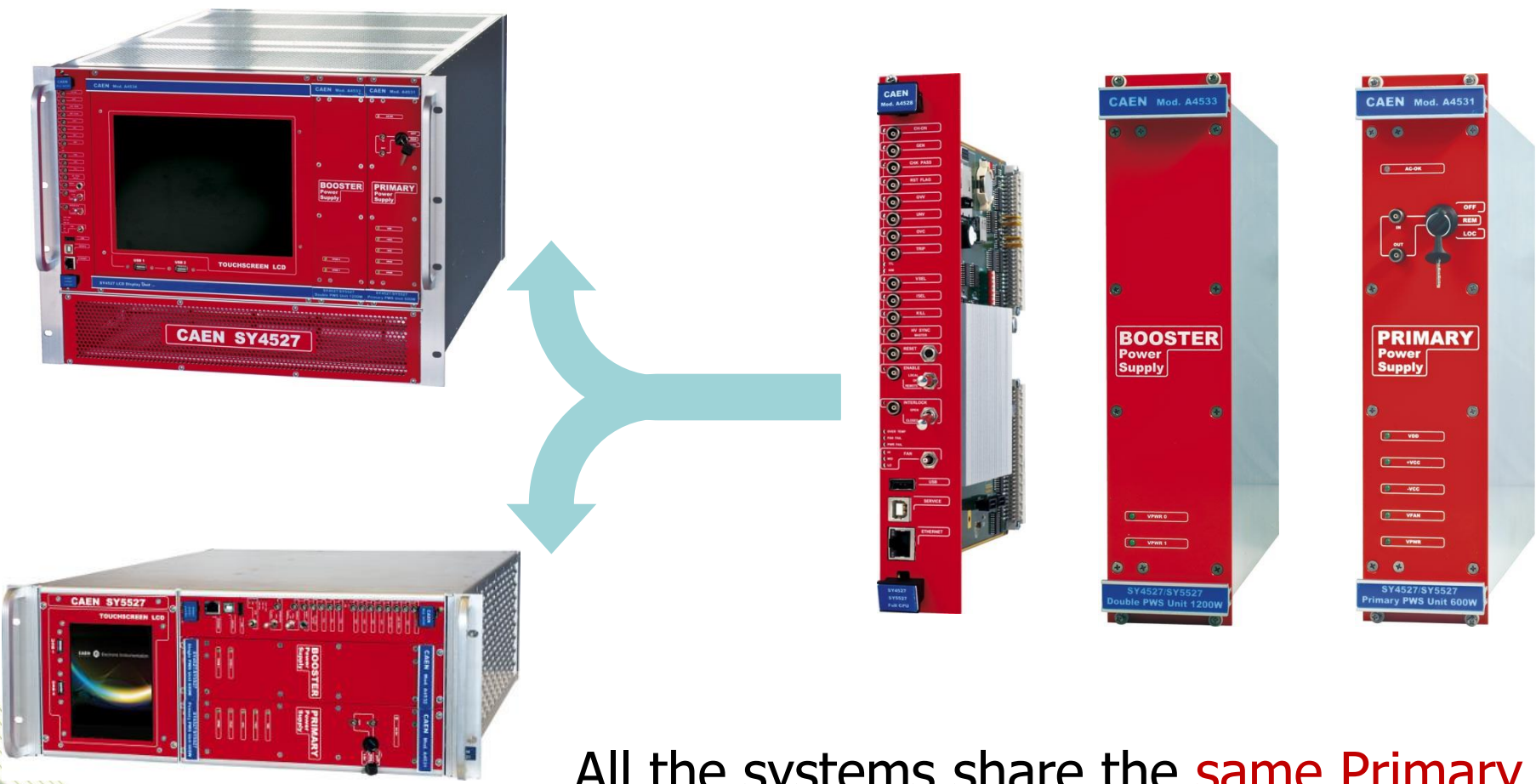
Usability

- New **Software** tools have been designed to set and monitor all the parameters. **Advanced features** for **Alarming**, **Logging** and **Scripting**

Compatibility

- The new backplane is **fully compatible** with **SY1527/2527** HV/LV Boards and Branch Controllers

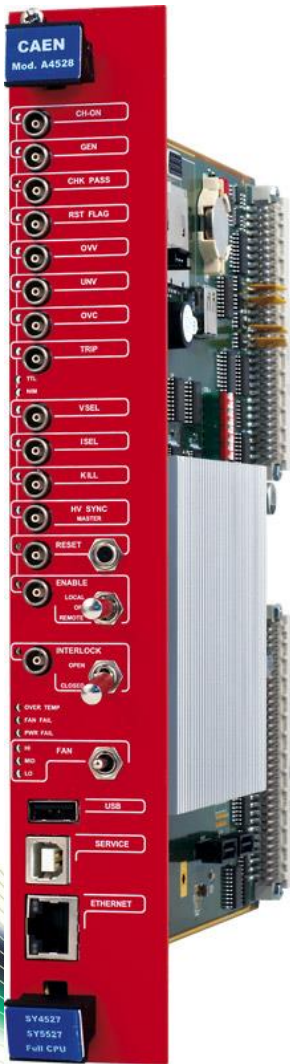




All the systems share the **same Primary Power Supply**, the **same Boosters** and the **same CPUs**

- ✓ A4528 Built-in industrial PCs
 - **Ethernet** (TCP/IP) connection
 - **Wireless** connection through Wi-Fi USB dongle
- ✓ Local control via **Touchscreen LDC**
- ✓ Control software for Linux, Windows and Tablet PC
- ✓ User profiles & View Customization





✓ Basic version

- communication interfaces
- RESET control
- INTERLOCK control
- Status LEDs

✓ Advanced version adds:

- beam handshake management connectors (CH-ON, GEN, VSEL, ISEL)

✓ Full version adds:

- complete set of panel connectors
- ENABLE control section
- Front panel Fan speed control.

GECO2020

General Control Software for CAEN HV Power Supplies



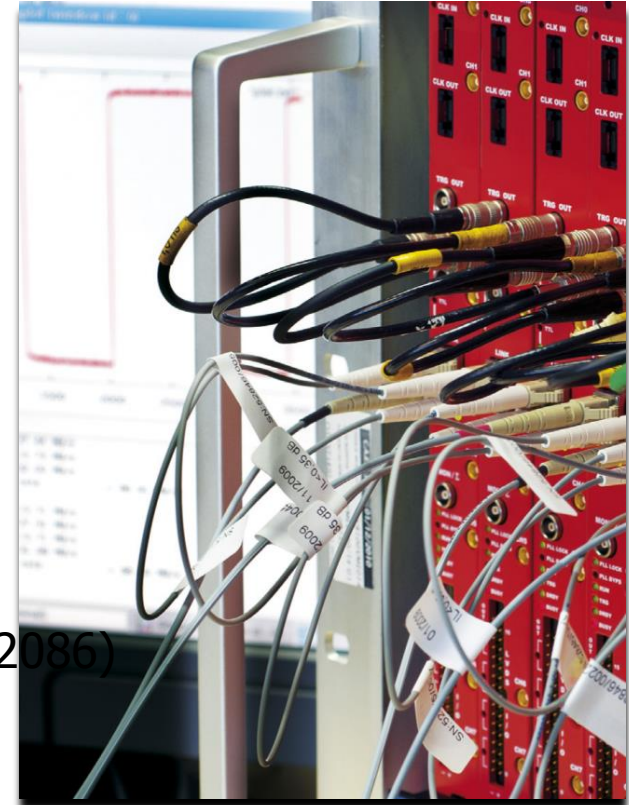
- ✓ Innovative GUI
- ✓ Dashboard capability: allows to manage all the CAEN Power Supplies in any form factor
- ✓ Supports Linux and Windows
- ✓ Handles all the communication links: Ethernet & Wi-Fi, USB, Optical Link

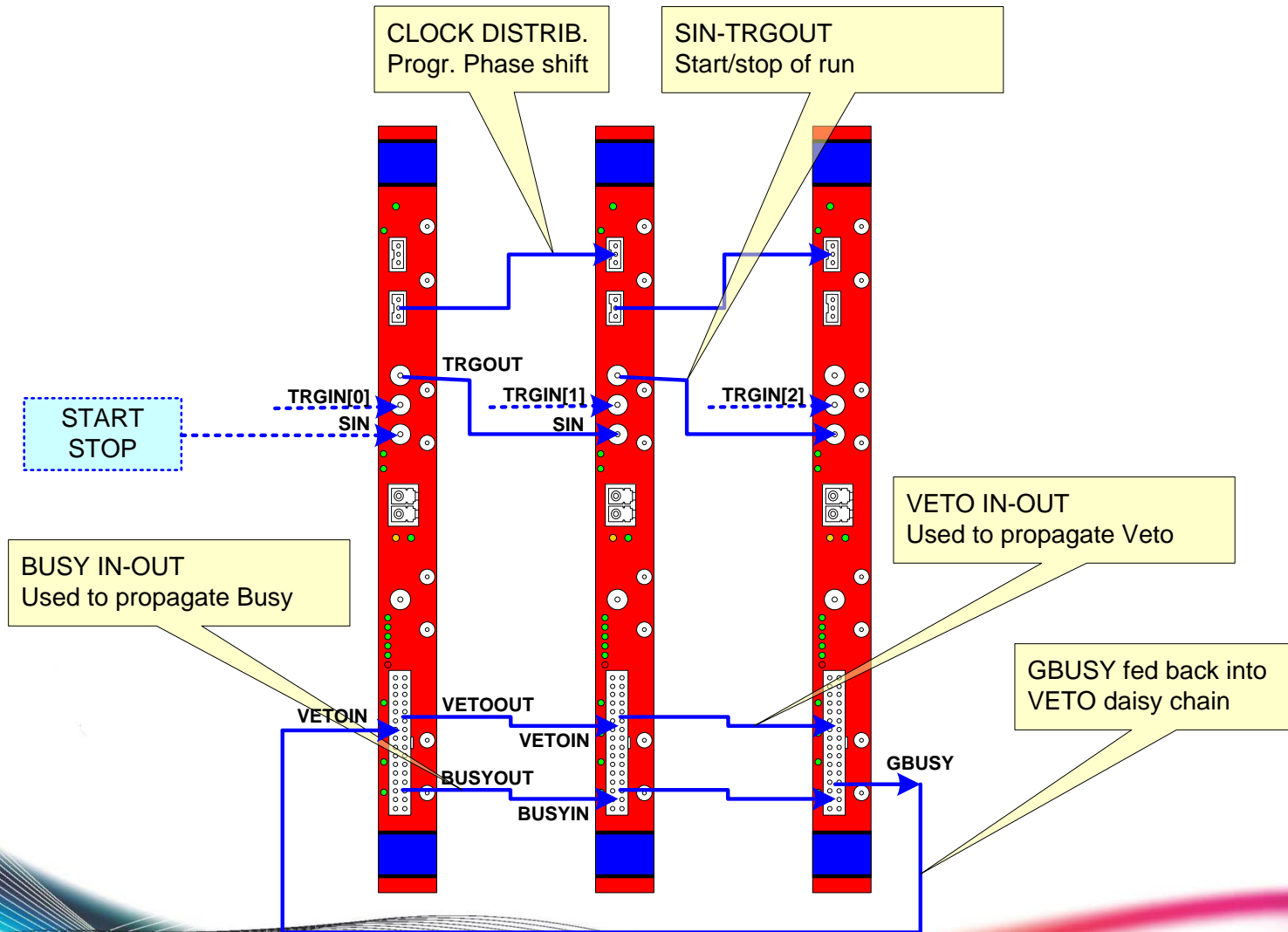
Channel	Name	ISet	VSet	IMon	VMon	Pw	Status
09.000	CHANNEL00	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.001	CHANNEL01	900.00 uA	100.0 V	0.15 uA	0.0 V	Off	
09.002	CHANNEL02	900.00 uA	100.0 V	0.00 uA	0.0 V	Off	
09.003	CHANNEL03	900.00 uA	100.0 V	0.20 uA	0.0 V	Off	
09.004	CHANNEL04	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.005	CHANNEL05	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.006	CHANNEL06	900.00 uA	100.0 V	0.05 uA	0.0 V	Off	
09.007	CHANNEL07	900.00 uA	100.0 V	0.00 uA	0.0 V	Off	
09.008	CHANNEL08	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.009	CHANNEL09	900.00 uA	100.0 V	0.15 uA	0.0 V	Off	
09.010	CHANNEL10	900.00 uA	100.0 V	0.00 uA	0.0 V	Off	
09.011	CHANNEL11	900.00 uA	100.0 V	0.15 uA	0.0 V	Off	
09.012	CHANNEL12	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.013	CHANNEL13	900.00 uA	100.0 V	0.00 uA	0.0 V	Off	
09.014	CHANNEL14	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.015	CHANNEL15	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.016	CHANNEL16	900.00 uA	100.0 V	0.15 uA	0.0 V	Off	
09.017	CHANNEL17	900.00 uA	100.0 V	0.15 uA	0.0 V	Off	
09.018	CHANNEL18	900.00 uA	100.0 V	0.05 uA	0.0 V	Off	
09.019	CHANNEL19	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.020	CHANNEL20	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	
09.021	CHANNEL21	900.00 uA	100.0 V	0.05 uA	0.0 V	Off	
09.022	CHANNEL22	900.00 uA	100.0 V	0.15 uA	0.0 V	Off	
09.023	CHANNEL23	900.00 uA	100.0 V	0.10 uA	0.0 V	Off	



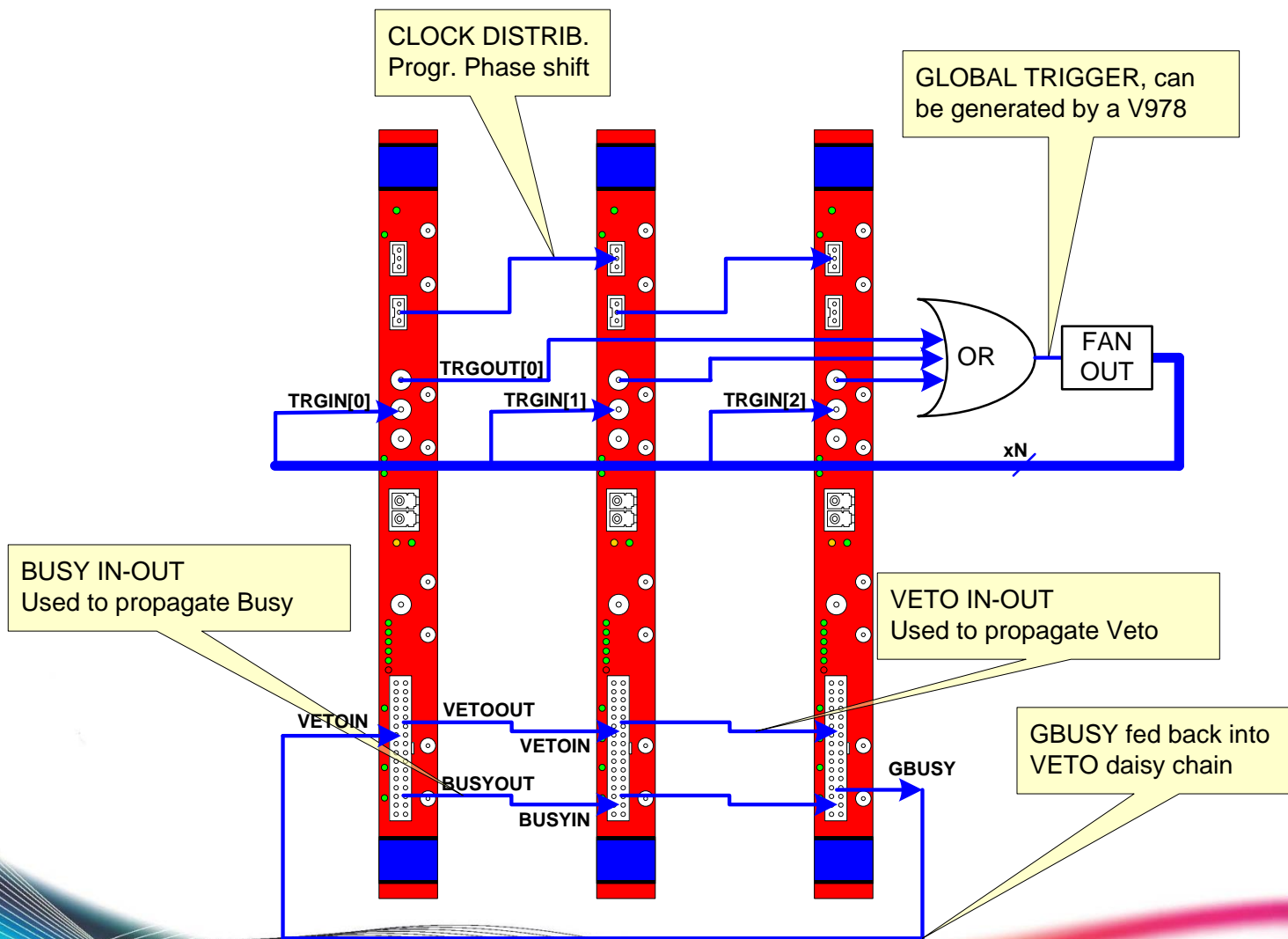
Board Synchronization

- Basics
 - Clock phase-aligned
 - Clock input/output, programmable phase adjust
 - Same time reference
 - Time stamp reset, input/output connectors
 - Trigger propagation and/or correlation
 - Possible use of external logic units
 - Readout synchronization and event alignment
 - Input/output to propagate BUSY or VETO signals
- Software demo:
 - **SyncTest** source code, ANSI C
 - **Application Note** with simple examples (AN2086)
- **Some examples** follow

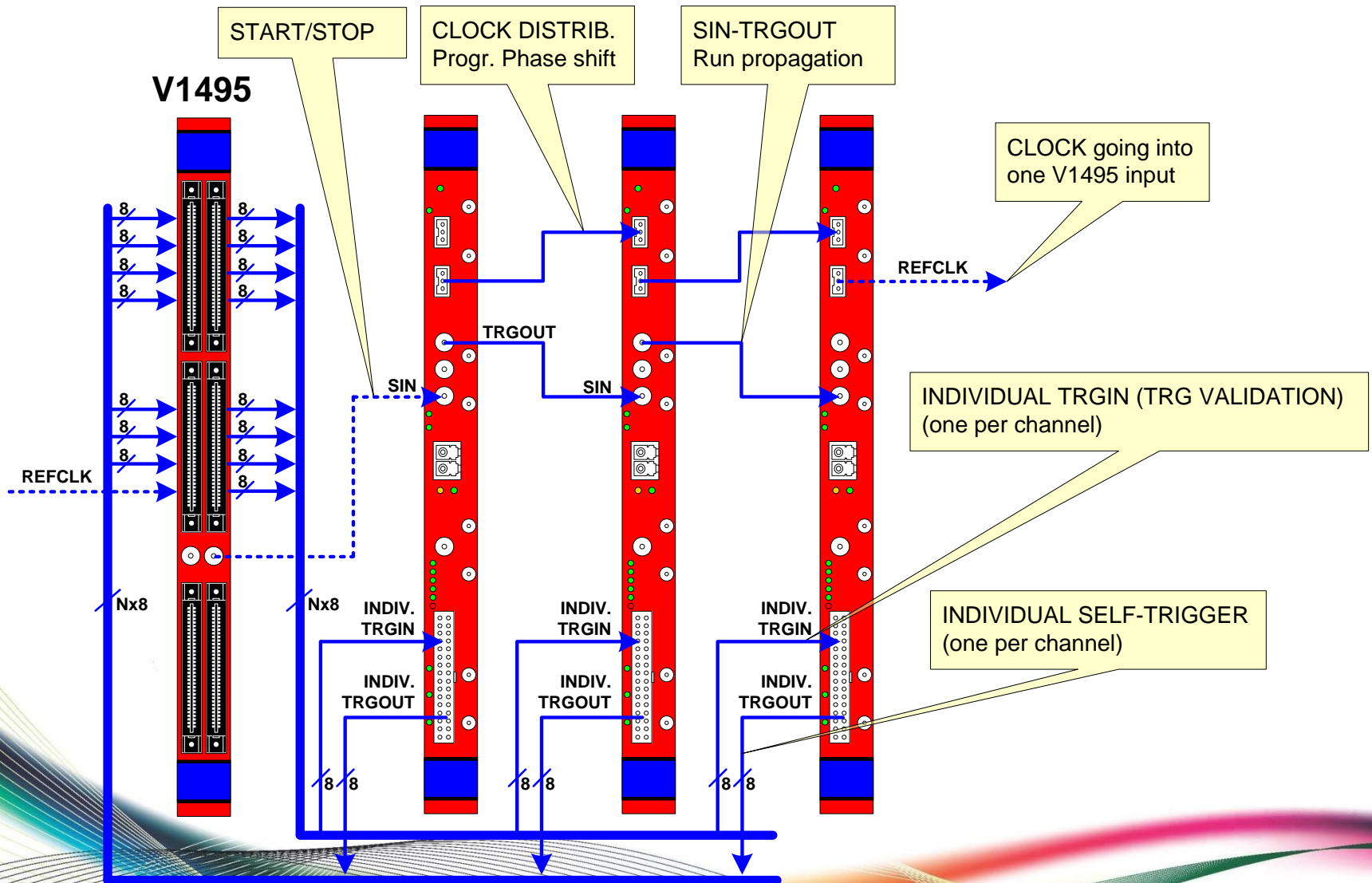




Multi-board Synchronization: example 2



Multi-board Synchronization: example 3

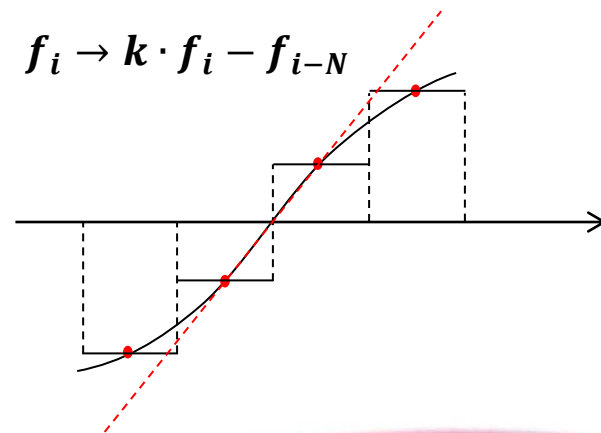
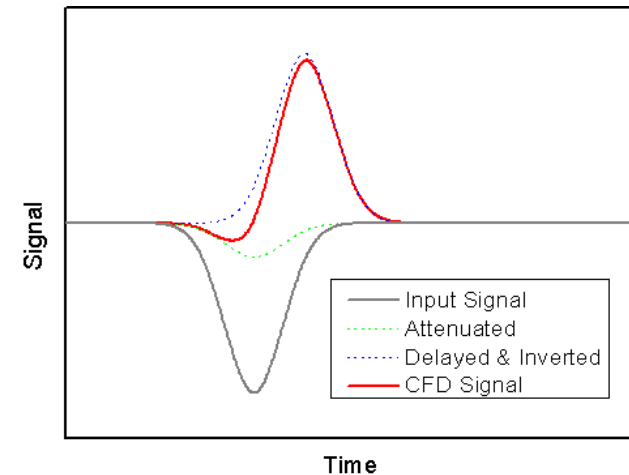


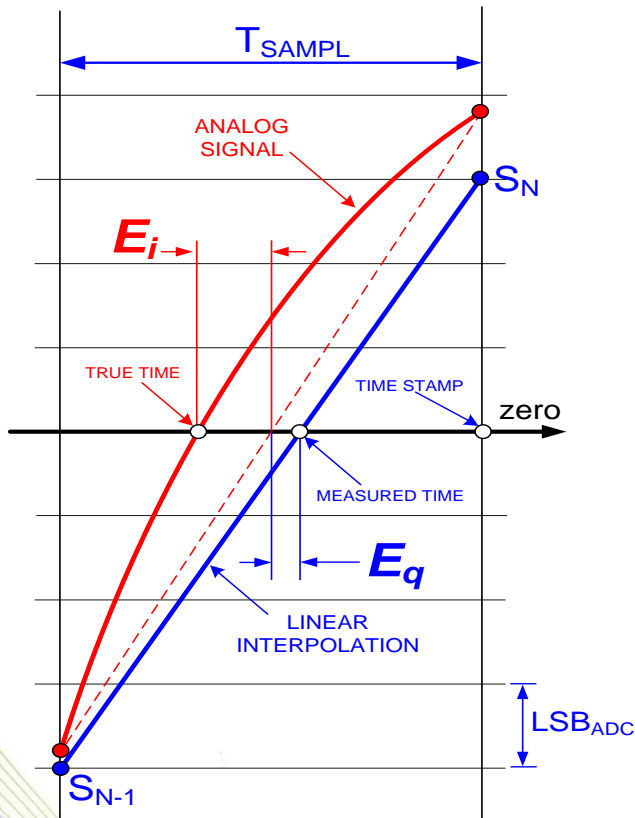
Digital CFD

Signal Processing for Time Measurement

- Best timing resolution may be obtained with interpolation algorithms
 - Need to read full waveforms
 - High data transfer rate compared to traditional TDC
- As for the analog systems, high precision timing may be obtained with Constant Fraction Discriminators
 - solve the "amplitude walk"
- On-line FPGA processing may help, but the algorithm has to be simple
 1. implement the CFD with online algorithms
 2. find the zero crossing with resolution of the sampling clock
 3. interpolate the points to improve significantly the result

$$f(x) \rightarrow k \cdot f(x) - f(x - \Delta t)$$





There are two types of error (excluding noise):

Quantization error E_q

Interpolation error E_i

- **Slow signals** (Rise Time $> 5 \cdot T_s$): $E_i < E_q$

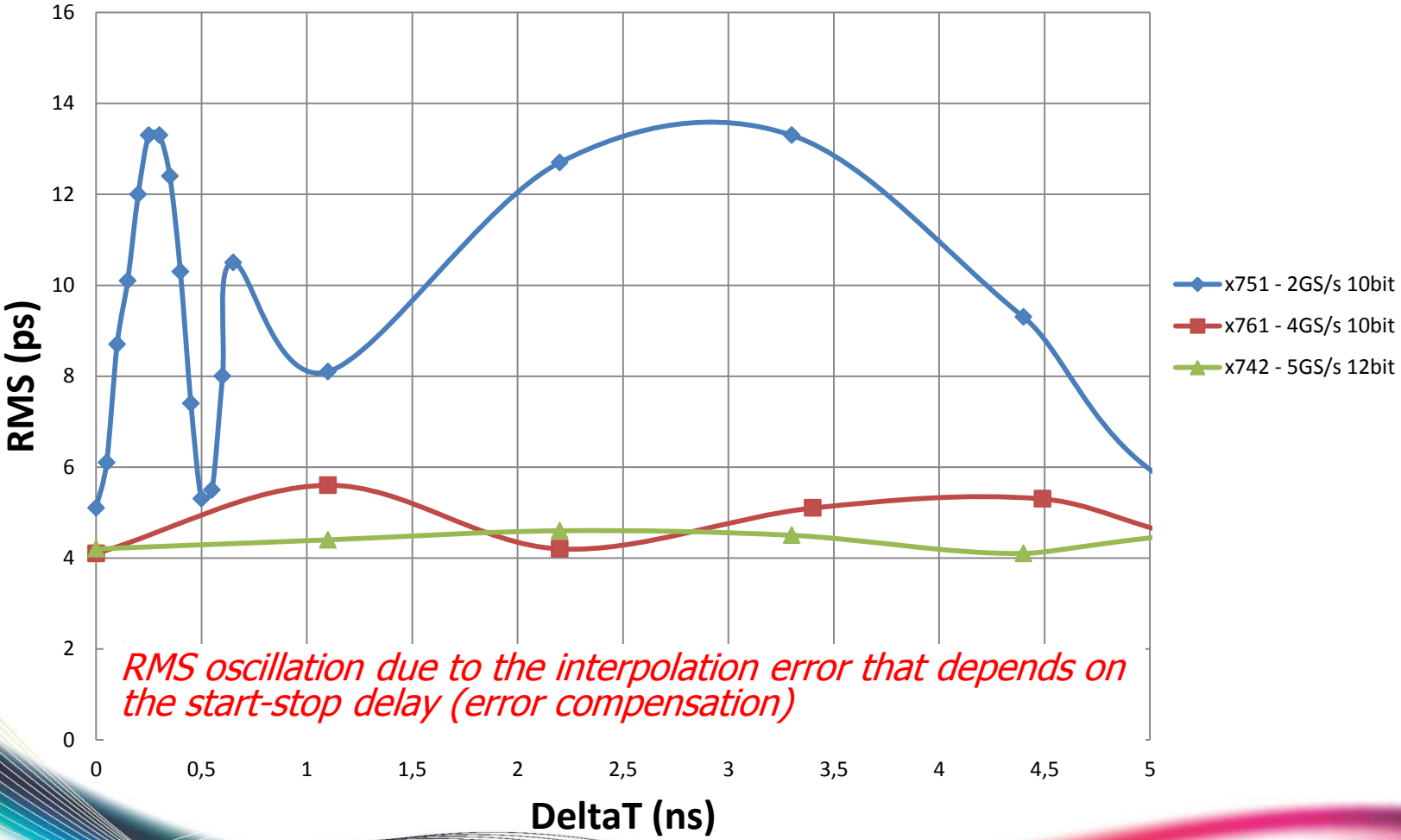
Approximation to a straight line is good; resolution proportional the number of bits of the ADC and to the rise time

- **Fast signals** (Rise Time $< 5 \cdot T_s$): $E_q < E_i$

The geometric error due to the interpolation varies with the position of the signal respect to the clock, thus giving non gaussian peaks and other non-physical effects.

RMS vs DeltaT @ 0.8ns Rise Time, 1V

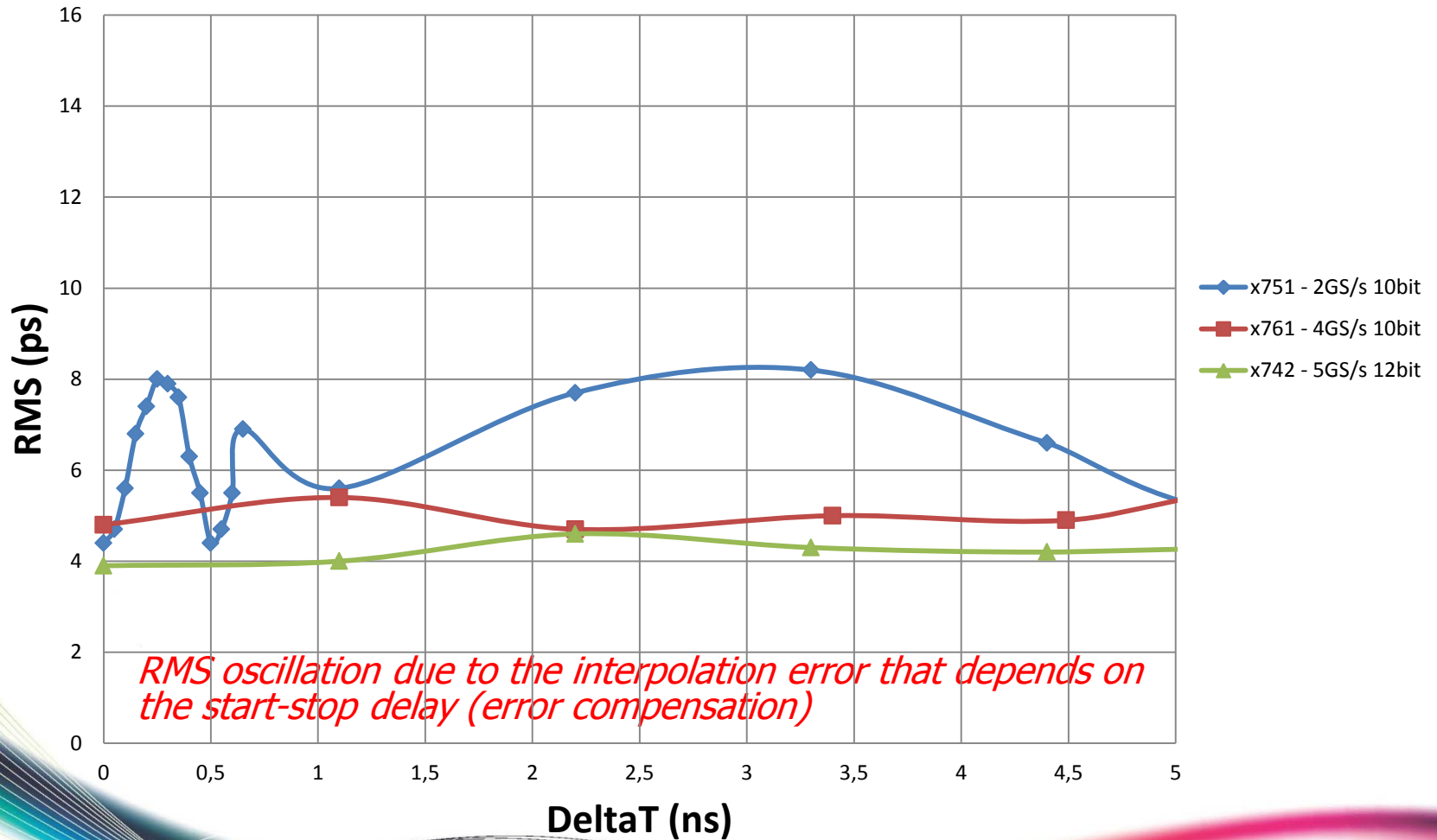
Amplitude = ~1V, Edge = 0.8 ns



RMS oscillation due to the interpolation error that depends on the start-stop delay (error compensation)

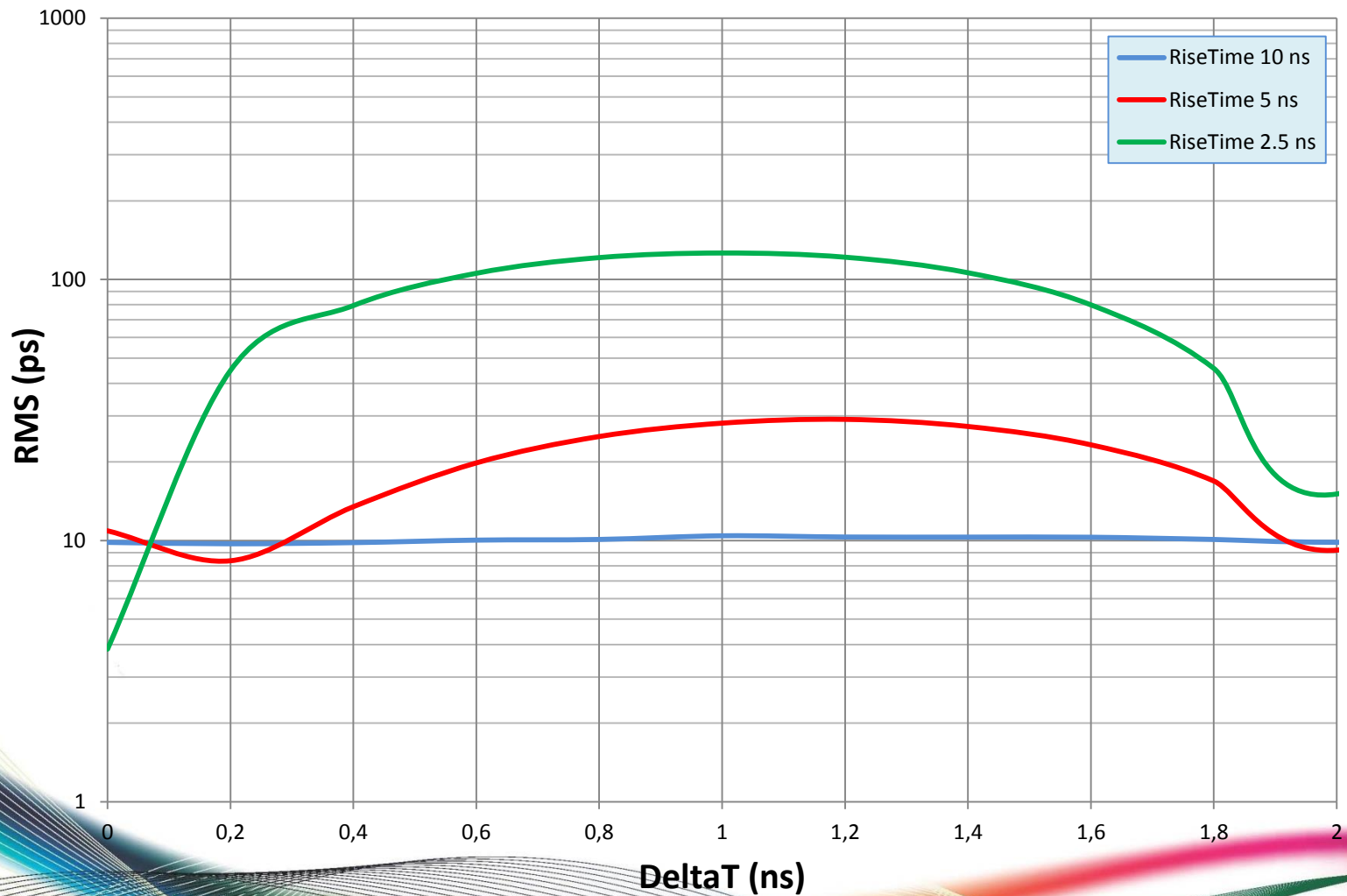
RMS vs DeltaT @ 1.6ns Rise Time, 1V

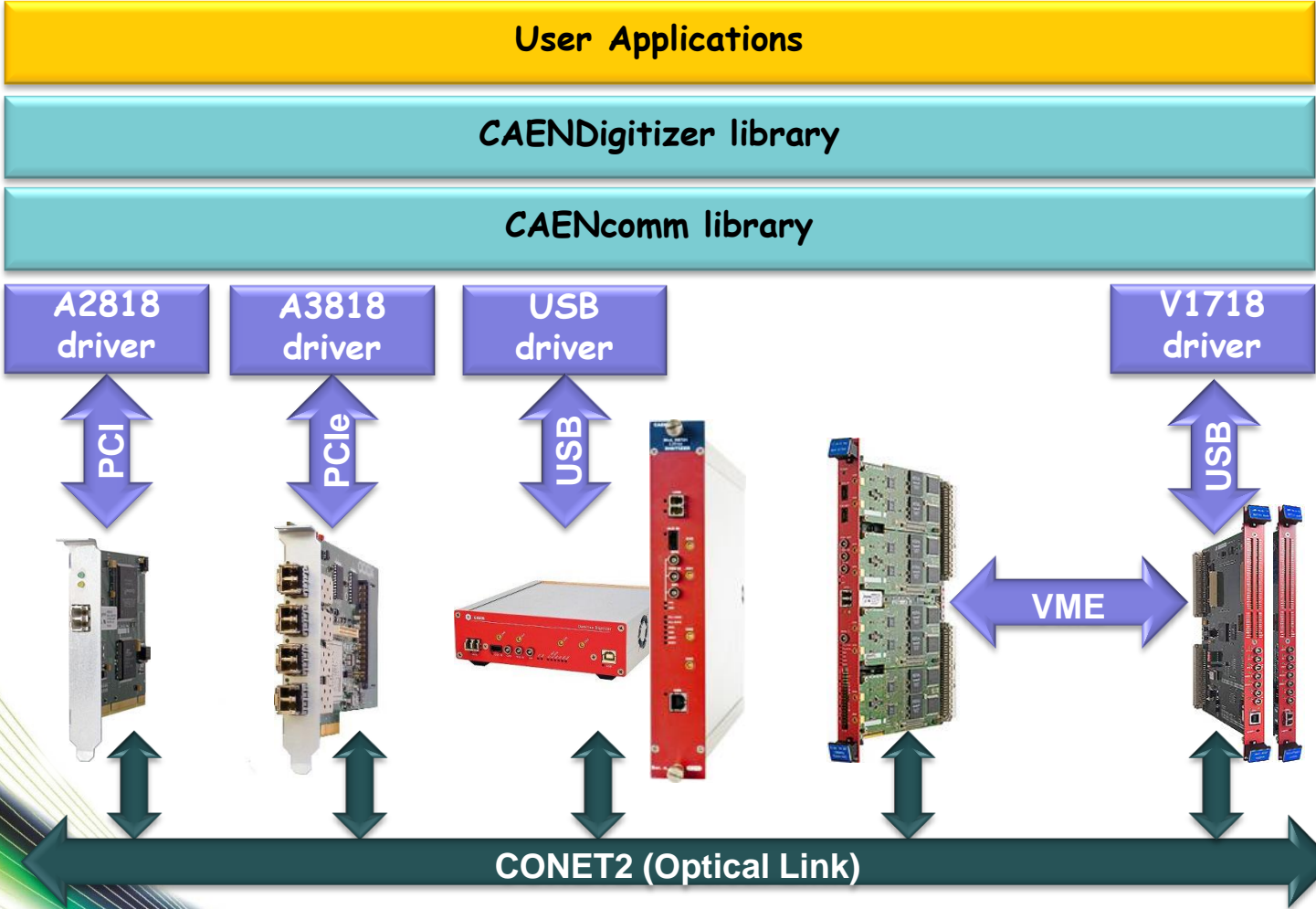
Amplitude = ~1V, Edge = 1.6 ns



Beta test with x730 (14 bit, 500MS/s)

Amplitude = 1 V





Set/Get Params,
Start/Stop Read Events,
etc.

Open/Close, Read, Write